IN THE CLAIMS

1. (Previously presented) An electrically erasable programmable memory device, comprising:

a first semiconductor layer doped with a first dopant ~~in~~ at a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

a first diffusion region and a second diffusion region embedded in the top side of the second semiconductor layer and defining a channel region therebetween, each diffusion region being doped with the first dopant ~~in~~ at a second concentration greater than the first concentration;

a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate being capable of storing electrical charge; and

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate and separated therefrom by a first vertical insulator layer, wherein the control gate is adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region, and wherein the control gate and the floating gate share a planarized top surface.

2. (Previously presented) The memory device of claim 1, wherein the first dopant has a P-type characteristic and the second dopant has an N-type characteristic.

3. (Previously presented) The memory device of claim 1, wherein the first dopant

has an N-type characteristic and the second dopant has a P-type characteristic.

4. (Previously presented) The memory device of claim 1, wherein the first insulator region has a thickness that allows tunneling of charge between the floating gate and the first channel region.

5. (Original) The memory device of claim 4, wherein the thickness is between 70 angstroms and 110 angstroms.

6. (Previously presented) The memory device of claim 1, wherein the vertical insulator is made from a silicon dioxide having a thickness that prevents leakage between the floating gate and the control gate.

7. (Previously presented) The memory device of claim 1, wherein the first vertical insulator is made from an oxide-nitrite-oxide material having a thickness that prevents leakage between the floating gate and the control gate.

8. (Original) The memory device of claim. 1, wherein the floating gate and the control gate are wrapped by a spacer.

9. (Original) The memory device of claim 1, wherein the second diffusion is in contact with a vertical connector, the vertical connector being separated from the control gate by a second vertical insulator.

10. (Previously presented) The memory device of claim 9, wherein charge is transported from the first channel region to the floating gate when a first combination of voltages are applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

11. (Previously presented) The memory device of claim 10, wherein the first

combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the second semiconductor layer;

applying a positive high voltage to the first diffusion region;

applying zero voltage to the second diffusion region; and

applying to the control gate a decreasing positive voltage over a first time period, followed by an increasing voltage over a second time period.

12. (Previously presented) The memory device of claim 10, wherein the first combination of voltages are applied according to a method which comprises:

applying a positive voltage between 1V and a programming voltage to the control gate;

applying a zero voltage to the first diffusion region;

applying a positive high voltage to the second diffusion region; and

applying a positive voltage between 0V to a supply voltage to the second semiconductor layer.

13. (Previously presented) The memory device of claim 9, wherein charge inside the floating gate can be determined when a first combination of voltages ~~is~~ are applied to the first diffusion region, the control gate, and the second semiconductor layer.

14. (Previously presented) The memory device of claim 13, wherein the first combination of voltages are applied according to a method which comprises:

applying a supply voltage to the second semiconductor layer;

applying a supply voltage to the first diffusion region; and

applying a voltage between -2V and the supply voltage to the control gate.

15. (Original) The memory device of claim 1, wherein the first diffusion is in contact with a vertical connector, the vertical connector being separated from the floating gate by a second vertical insulator.

16. (Previously presented) The memory device of claim 15, wherein charge is transported from the first channel region to the floating gate when a second combination of voltages are applied to the first diffusion region, the control gate, and the second semiconductor layer.

17. (Previously presented) The memory device of claim 16, wherein the second combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a supply voltage to the second semiconductor layer.

18. (Original) The memory device of claim 16, wherein the second combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a negative voltage to the second semiconductor layer.

19. (Previously presented) The memory device of claim 1, wherein charge is

transported from the floating gate to the first channel area when a third combination of voltages are applied to the second semiconductor layer, the control gate, and the first diffusion region

20. (Previously presented) The memory device of claim 19, wherein the third combination of voltages are applied according to a method which comprises:

applying a negative voltage to the control gate;

applying a high positive voltage to the second semiconductor layer; and

applying a positive high voltage to the first diffusion region.

21-49. (Canceled)